Investigations into the Power MOSFET SEGR Phenomenon and Its Physical Mechanism

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INTRODUCTION

The state of understanding of the destructive SEGR event in power MOSFETS is relatively mature with large published efforts, both experimental [1-5] and theoretical [6-8]. However, gaps remain in the understanding of the phenomenon, including unexplained experimental anomalies, empirical-only dependencies on some important device and incident ion physical parameters, and limited insight into latent effects. This paper's purpose is to shed light on some of these using a selected range of real-world devices. In subjecting these devices to the usual accelerator experiments, during-irradiation current signatures were anal yzed for the first time. To augment the heavy ion experiments, doping profiles and gate oxide thicknesses were measured and PISCES-based analyses were performed, Finally, post-SEGR failure investigations were conducted. These results yield new parametric correlations and physical insights into the SEGR failure mechanism.

EXPERIMENTAL RESULTS

Test devices from two manufacturers, Harris and International Rectifier (INR), were obtained from commercial sources, with voltage ratings from 100 to 400 V. These were not total dose hardened. For comparison, JANTXV 100 krad(Si) hardened devices (suffix R3) were also tested, and gave the same gate rupture results as the more ordinary devices (suffix D 1). The test devices were irradiated using four normally incident ion species accelerated by the Texas A&M University cyclotron with ranges from 120 to 185 microns so that range issues [9] were eliminated. The remarkable consistency of depletion mode rupture points in V_{DS}-V_{GS} space (when irradiated with a sufficient fluence) noted by previous experimenters [2] was also seen here and used to reduce the need for multiple samples of a given point. Shown in Figure 1, these results are consistent with later Titus and Wheatley results [1,9] with production devices showing non-linear contours, rather than the earlier more nearly linear results [2,4] obtained, in some cases, with specially formulated test devices. Note that not only are the failure points shown, but also the highest applied voltage for which the device under test did not fail in order to give the resolution of each data point. Also, note that several of these points arc "latent" failures which are discussed below.

While Figure 1 shows the measured minimum combinations of V_{GS} and V_{DS} needed to cause gate rupture for ions of two LETs for the 200 V Harris devices, Figure 2 gives similar results for the 100 V INR device as a function of LET, after Ref. 7. Both presentations include points for the highest V_{DS} irradiated without failure (the open symbols). A comparison of the two manufacturers' devices shows that from an SEGR standpoint the INR devices are harder. Full data sets for the five device types will be presented in the full paper.

Part-to-part variation is inherent in SEGR testing because each data point is for a distinct sample, so the consistency of the failure points is a testimony not only to the uniformity of the manufacturing process, but also is reflective of a sharp "edge" to the failure region in the physical mechanism given a particular device construction. The main features of the vertical power MOSFET structure are shown in Figure 3, with the exception of the gate oxide itself (between the gate poly and the underlying epi) because it is too thin to be shown on this scale. A simulation (using PISCES), on a simple cylindrically-symmetric oxide-semiconductor structure representing the neck region of a generic 300V MOSFET with 20 μm epi and 100 run oxide, produced a plot of potential vs. depth along the ion track shown in Figure 4. The electric field (the slope of the curve) in the gate oxide is much larger at 20 ps after a simulated ion hit than it was prior to the hit, with the potential across the oxide exceeding 80 V. A limitation of PISCES is that it cannot predict currents after the oxide begins to break, and thus does not help with the oxide rupture mechanism. Similar simulations reflecting actual device physical parameters (oxide and epi thicknesses and doping) and experimental LETs will be conducted in the full paper. Towards that

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end, spreading resistance (for the device doping profiles) and gate oxide thicknesses *were* measured and are summarized in Table I.

Table I. Physical Measurements of the Test Devices

	rated V_{DS} *max.*	*gate oxide* (rim)	*epi* (μm)
INR 2N6782	100V	7533	15
INR 2N6790	200 v	75 ±5	26
INR 2N6786	400 v	75 ±5	40
Harris FRL130	100V	46+4	20
Harris FRL230	200 v	57 ±3	19

Interestingly, the two manufacturers have taken different approaches to making the higher voltage devices. INR uses the same oxide thickness, changing mainly the doping depth (cpi thickness), while Harris varies the oxide thickness with some tailoring of doping levels, but with essentially the same epi thickness. With full rated voltages applied, practically the entire lightly doped epi region is depleted for all these devices. Given a relatively linear potential profile, like that of the pre-strike curve in Figure 4, the increased epi thickness that accompanies increased voltage results in comparable electric fields for all three INR devices. This facilitates the comparison of their SEGR responses, because it removes differences in the pre-strike field shape. Additionally, since the oxides are the same, the minimum sum of V_{GS}-applied and V_{GS}-transient needed to cause SEGR should be constant. Under the additional assumption that the fraction, η, of V_{DS} that appears as the gate transient is constant for a given LET, the VGS-VDS points for threshold conditions (like those of Figure 1) should be approximately linear. Fitting two of the INR devices under this simple approximate ion yields a critical V_{GS} sum of about 45 V and the η function shown in Figure 5. The fit of Figure 5 is reasonably good, but the planned PISCES simulations will yield individual η values for each device-V_{DS}-LET combination, improving the fit.

While the transient created by the ion adds to the effective gate bias and is clearly an important part of most SEGRs observed, it does not take into account that damage to the oxide is also a necessary part of the mechanism. Three experiments illustrate the point. First, Wrobel's pioneering work on dielectric "errors" [10] used MOS capacitor structures biased in both directions. Second, similar destructive effects have been observed in commercial devices with structures that clearly do not have biased underlying silicon [11,12]. Further, the MOSFET experiments themselves are sometimes conducted with V_{DS}= O V and ion-induced gate rupture occurs. For example, note the point in Figure 1 with V_{DS}= O V. Clearly then, the V_{DS} transient is not needed to cause gate rupture, although it does lower the required static oxide bias.

Other evidence of weaknesses in the understanding of the SEGR mechanism were revealed by these experiments. The electrical characteristics of the resulting damage vary; while most end up as resistive shorts between the gate and source (or source and drain, in some cases), a few events show a gatedrain short, Also, strip charts of the currents during the irradiation sometimes show an exceptional signature. Figure 6 shows an unusual signature in the gate current. Normally, a sudden catastrophic gate current at or near the supply limit (60 mA, in this case) suddenly appears. In this case, a small gate current (-1 O μA) appears while irradiating with VDs = 65 V, disappears when V_{DS} is stepped, but reappears during the following irradiation. Finally a clear, large (non-disappearing) current begins to flow after two more V_{DS} steps and irradiations. Other odd during-beam and post-failure signatures were collected, and a full understanding of the SEGR mechanism would explain these. While it is possible that these are merely differences in the way the damage accrues after the actual SEGR event, it is more likely that they are important mechanism clues.

Additionally the appearance of "latent" or "delayed" SEGR as noted by some experimenters [2,5] shows that SEGR"... does not (necessarily) depend upon a simultaneous interaction of applied field and the deposited ionized charge," [5]. In fact, in the present data set approximate y 10°/0 of the data points were observed during the VDS= O V gate leakage measurement that was done between irradiations in preparation for stepping up in

bias or in the pre-beam measurement after V_{DS} was stepped. Both of these out-of-beam types of failures indicate that the fundamental damage to the oxide caused by the ions had already occurred. This means that not only is the oxide damage a necessary component of gate rupture, but that the damage is not a fast transient effect (a temporary weakness, for instance) on the time scale of the ion passage.

Finally, under the transient bias model, each ion that hits the neck region and is capable of causing a gate rupture, should do so [6-8]. Some experimenters have shown data with a match between neck area and SEGR cross section [1, 13]. However, Fig. 5 of Ref. 7 has an order of magnitude disagreement with Fig. 12 of Ref. 1 for the same device, ion, and bias conditions. One possible explanation is related to the "delayed" ruptures. If a short time latency is usual (although that would be quite surprising), additional fluence would be counted between the time of the damage and its observation. The extra fluence would be less if the flux were lower. Consistent with this notion is the fact that Ref. 1, which reported the high cross section noted above, used an unusually low flux of about 25 ions/sec/cm^2 ; Ref. 7 does not document the flux used, but ordinarily it's about two orders of magnitude higher. Clearly more investigat ion is warranted.

CONCLUSIONS

The modeling of SEGR has concentrated on the collapsing of part of the vertical V_{DS} field (across the semiconductor region) which adds to the applied V_{GS} for a short time during the ion strike increasing the field across the gate oxide. Much of the present work supports (or the interpretation depends on) the essential validity of this viewpoint. PISCES (and other physics simulation tools) along with the measured doping profiles ean contribute to the understanding of the evolution and relative size of the added field and the full paper attempts to add to that understanding. However, such tools are not yet able to show the oxide breakdown mechanism itself, and existing models are merely empirical fits to the SEGR data (usually assuming a fixed minimum oxide breaking voltage) the collapse of the depleted region in the lightly-doped silicon does not address the oxide breakdown mechanism itself. Experimental evidence presented here demonstrates that the current picture is incomplete. From the "latent" failures, it appears that SEGR is a two (or more) step process where the ion strike may initiate the failure, but gate bias completes the oxide punch-through. The fact that the gate bias may be applied long after the strike and be well within the maximum V_{GS} rating lowers the importance of the transient field; from this viewpoint, it only facilitates the appearance of catastrophic damage, but is not a primary cause of the rupture. Additionally, the resultant physical darnage is not as consistent as the model literature implies, as can be seen in the irradiation current strip charts. These observations, together with appropriate information about the test devices' physical parameters, can lead to a more complete understanding of the SEGR phenomenon.

REFERENCES

[1] C.F. Wheatley et al., "SEGR Response of a Radiation-Hardened Power MOSFET Technology," *TNS*, p. 2944, Dec. 1996.

[2] J.L. Titus and C.F. Wheatley, "Experimental Studies of Single-Event Gate Rupture and Burnout in Vertical Power MOSFET's," *TNS, p.531,* April 1996; and extensive references therein.

[3] H.M. Joseph, "Radiation-Induced Effects on Special Super Large N-Channel MOSFETs for Space Applications," *RADECS Proceedings,* p. 128, 1991.

[4] J. Titus et al., "Impact of Oxide Thickness on SEGR Failure in Vertical Power MOSFETs: Development of a Semi-Empirical Expression; *TNS,* p. 1928, Dec. 1995.

[5] D.K. Nichols et al., "Single Event Gate Rupture in Commercial Power MOSFETs," *RADECS Proceeding,* 1993.

[6] G.H. Johnson, et al., "A Review of the Techniques Used for Modeling Single-Event Effects in Power MOSFET's," p. 546, April 1996 and extensive references therein.

[7] M. Allenspach, et al., "SEGR and SEB in N-Channel Power MOSFETs," *TNS*, p. 2927, Dec. 1996,

[8] G.H. Johnson et al., "A Physical Interpretation for the Single-Event-Gate-Rupture Cross-Section of N-Channel Power MOSFETs," *TNS, p. 2932,* Dec. 1996.

[9] J. L. Titus et al., "Influence of Ion Beam Energy on SEGR Failure Thresholds of Vertical Power MOSFETs," TNS, p. 2938, Dec. 1996

[10] T. Wrobel, "On Heavy Ion Induced Hard Errors in Dielectric Structures," 7NS, p. 1262, Dec. 1987.

[11] G. Swift and R. Katz, "An Experimental Survey of Heavy Ion Induced Dielectric Rupture in Actel Field Programmable Gate Array s," *RADECS* Proceedings, 1995.

[12] K. LaBel et al., "SEU Tests of... EEPROM Devices . . . ," *IEEE Radiation Effects Data Workshop,* p. 1,1992

[13] I. Moret et al., "Measurement of a Cross-Section for Single-Event Gate Rupture in Power MOSFET's," *IEEE Elect. Dev. Lett., v. 17, p. 163,* April 1996,

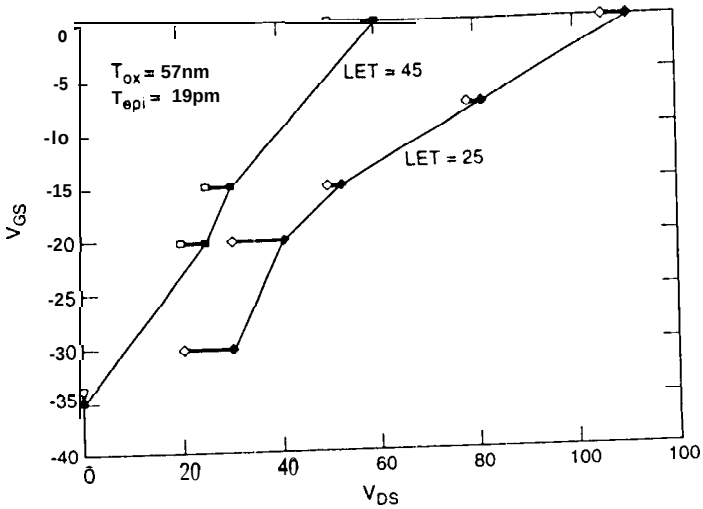

Fig. 1. Failure contours for tested LET values in V_{DS}-V_{GS} space for Harris FRL230's.

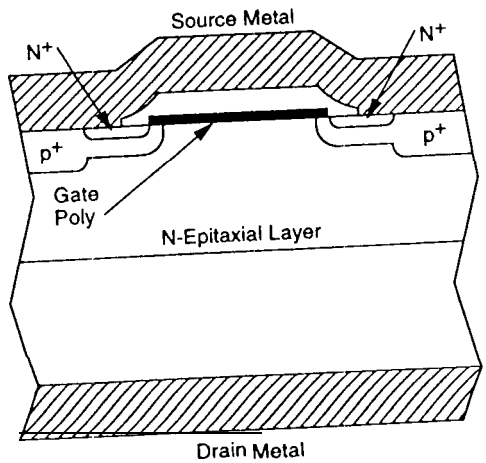

Fig. 3. Power MOSFET structure. The thin gate (not shown) lies between the gate poly and the n-epi.

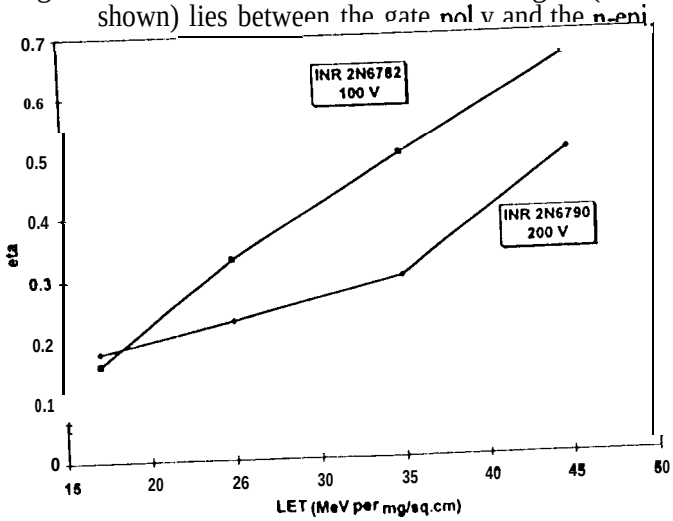

Fig. 5. The fitted efficiency of coupling V_{DS} onto the gate as a function of LET for two INR devices.

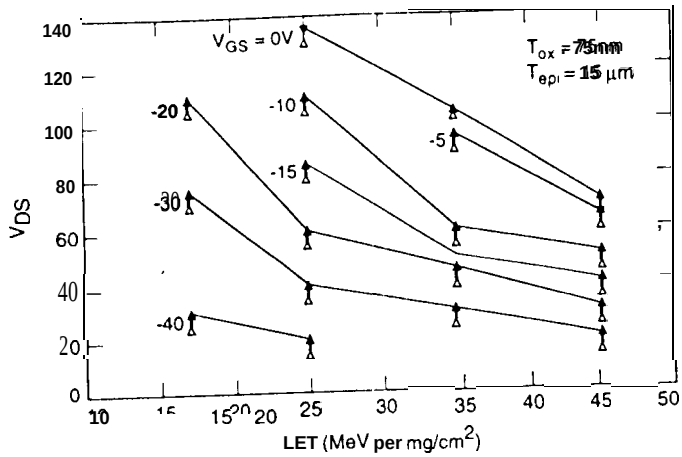

Fig. 2. Failure contours of V_{DS} as a function of LET for INR 2N6782 (100 V) devices.

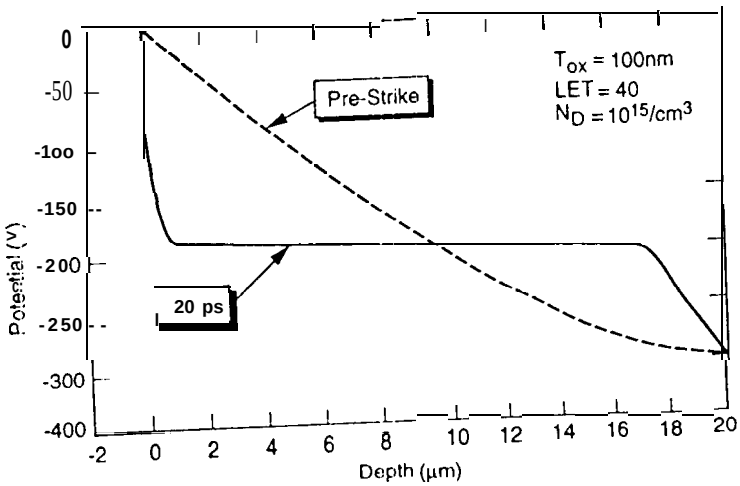

Fig. 4. Snapshot at 20 ps of PISCES simulation of field collapse contrasted to the pre-strike curve.

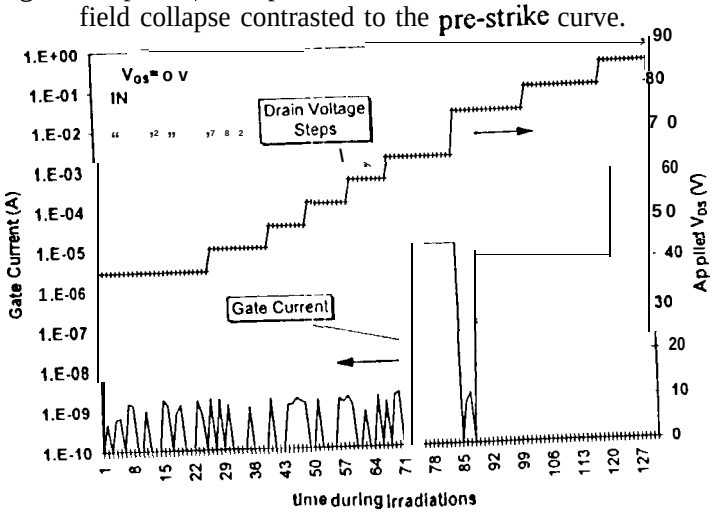

Fig. 6. SEGR signature of gate current during irradiation for two INR 2N6782's.